Apr 14 2020

Knowledge Check - VLSI SoC Design

5	5	0	0	100%	02:03
Questions	Right	Wrong	Unattended	Accuracy	Time Taken

5
Marks Scored

View rank list (https://elearn.maven-silicon.com/report/assessment/148)

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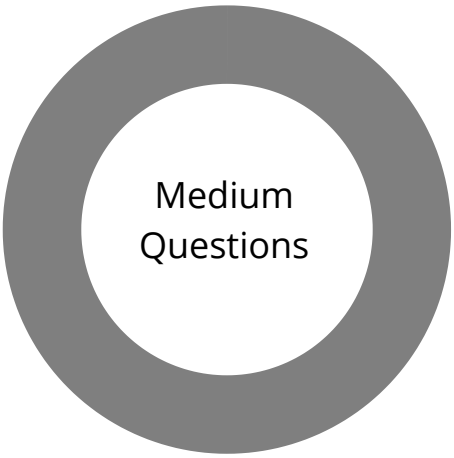
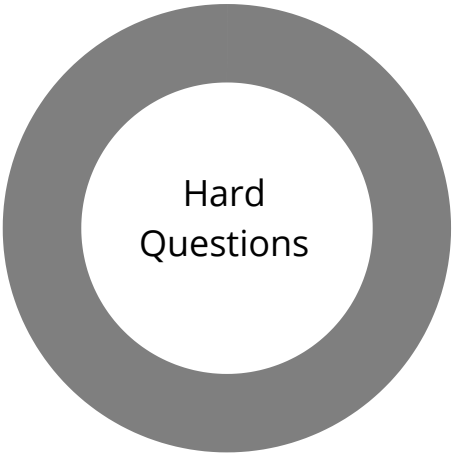
Topics	No.of Qns	Right	Wrong	Unattended	Accuracy	Remarks
Design Flow	5	5	0	0	100%	Excellent

Right Answers	5
Wrong Answers	0
Unattended	0



Right Answers	0
Wrong Answers	0
Unattended	0



Right Answers	0
Wrong Answers	0
Unattended	0

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All questions

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Showing **5** of **5** questions

1 Single choice

The design flow in VLSI Systems is in which order?

1. Architecture Design

2. Specification

3. Verification

4. HDL coding

a) **2 – 1 – 4 – 3**

b) **4 – 1 – 3 – 2**

c) **3 – 2 – 1 – 4**

d) **1 – 2 – 3 – 4**

e) **3 – 1 – 2 – 4**

Your answer (a) **Right** Time Taken **45s** **Marks 1** **Answer Explanation**

Based on specification, Architecture has to be designed. After this, HDL coding must b e done and it has to be verified.

2 Multiple choice

Placement and Routing process in the design flow can influence _____

a) **Speed of the circuit**

b) **Area occupied by the cir cuit**

c) **Power consumption**

d) **All of the above**

e) **None of the above**

Your answer (d) **Right** Time Taken **18s** **Marks 1** **Answer Explanation**

Depending on the place at which, you are placing different modules on the chip and de pending on the way, you are routing the interconnecting wires, the speed of the circuit, power consumption, area of the chip will be varied.

3 Single choice

IC's can operate at _____ and require the _____.

a) **lowest speed, largest die area**

b) **highest speed, largest die area**

c) **highest speed, smallest die area**

d) **lowest speed, smallest die area**

e) **None of the above**

Your answer C **Right** Time Taken **16s** **Marks 1** **Answer Explanation**

4 Single choice

The clock tree synthesis process is used for _____

a) **Increasing the clock slew rate**

b) **Increasing the speed of the circuit**

c) **Minimizing the clock skew effect**

d) **All of the above.**

e) **None of the above.**

Your answer C **Right** Time Taken **24s** **Marks 1** **Answer Explanation**

Because the differences in the lengths of clock distribution paths for various flipflops, clock skew will be existing between two flipflops in an IC. In order to minimize the sk ew, we use clock tree synthesis.

5 Single choice

Which 'law' describes the exponential growth of integrated circuit complexity?

a) **Nyquist's theorem.**

b) **Farday's law.**

c) **Moore's law.**

d) **Lenz's law.**

e) **None of the above**

Your answer (C) **Right** Time Taken **6s** **Marks 1** **Answer Explanation**

Gordon Moore has predicted that, the complexity of the chip grows and no. of transisto rs that can be fabricated on a single chip will be doubled for every 18 to 24 months.

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